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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/441,119	11/17/1999	OLIVER L. RICHARDS	ALLEG-017PUS	3874

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DALY, CROWLEY, MOFFORD & DURKEE, LLP
SUITE 101
275 TURNPIKE STREET
CANTON, MA 02021-2310

EXAMINER	
RAMAN, USHA	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/441,119	RICHARDS ET AL.	
	Examiner	Art Unit	
	Usha Raman	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed August 19, 2004 have been fully considered but they are not persuasive.

Applicant argues that "there is no motivation in the prior art to combine the cited references" because applicant's admitted prior art describes that the LNBP10 discloses reducing the power dissipation in the linear amplifier by using two voltage sources. However, the LNBP10 reference discusses two valid configurations of the LNB control and voltage regulator using one-voltage source with higher dissipation as well as two voltage sources with lower dissipation, depending on what the constraints of the applications are. What is lacking in the LNBP10 is the configuration of one voltage source with lower power dissipation. This feature is disclosed by Vizer, who teaches the step of using a switch mode power supply in order to use a single voltage supply to provide a plurality of voltage levels. Contrary to what the applicant argues, the modification of this does not teach away from the references because while the LNBP10 reference teaches lowering the power dissipation using two voltage sources, it lacks the benefit of lowering the power dissipation when using only one source. As stated in the non-final office action dated, July 7th, 2004, the motivation for such a modification is to provide a *single* voltage source capable of providing a plurality of output levels, thus *lowering power dissipation*, that is not otherwise possible using the standalone LNBP10 supply and control voltage regulator. Therefore, the examiner maintains the rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over "LNBP10 Series LNBP20" datasheet (henceforth referred to as LNBP10), published in September 1998 by ST Microelectronics in view of Vizer (US Pat. 5,893,023).

In regards to claim 1 and method claim 7, the LNBP10 datasheet describes a LNB supply and control voltage regulator circuit, comprising a linear amplifier means, which modulates a DC voltage level by an analog AC tone signal for providing power supply (from DC signal) and control (analog AC tone) signals to a remotely located LNB. The linear amplifier means further comprises a control port to which reference voltage indicative of the selected DC voltage level is applied (VSEL); and an input port for receiving a power supply output. The LNBP10 datasheet discloses that the power can be supplied from a single source supplying 23V or can be supplied from two sources supplying 16V and 23V each, where the VSEL controls the switching the two sources to supply the lowest supply voltage required, thus reducing the power dissipation. Note description in pages 1-2 and figure on page 5.

The LNBP10 requires two power supply sources for providing either 16V or 23V, depending on the required voltage as determined by the VSEL input to

the linear amplifier for reducing the power dissipation. The LNBP10 also allows the use of only one source but lacks the ability to reduce power dissipation when using only one supply voltage.

Vizer teaches using a switch mode power supply in a receiver to provide different operating voltage levels required to power to a LNB at the antenna assembly to minimize thermal dissipation within the receiver. The switch mode power supply comprises an input 6, connected to a DC voltage, an output 7. A voltage is delivered to the control input 13 for driving the base of the transistor and therefore the voltage delivered to the control input controls the operation of the switch mode power supply generating an operating voltage of the desired value. Note abstract, column 2, lines 5-21 and column 1, lines 47-53 of Vizer.

It would have been obvious to modify the LNBP10 circuit in view of Vizer's teachings to include a switch mode power supply in order to provide different operating voltages from a single DC voltage source, where the input of the switch mode power supply is connected to the single supply voltage source, and the control input of the switch mode power supply is coupled to VSEL, in order to regulate the output delivered to the linear amplifier means. The motivation would be to modify the LNBP10 circuit so it uses only one source with reduced power dissipation at the receiver, as taught by Vizer.

In regards to claim 2 and method claim 8, the satellite receiver comprises a low noise block converter of a satellite television system. Note column 1, lines 20-26 of Vizer and description in column 1, page 1 of the LNBP10 datasheet.

In regards to claim 3 and method claim 9, the modified circuit of LNBP10 in view of Vizer's teachings comprises an oscillator for generating analog AC tone signals. Note column 2, in page 1 and page 2, column 1 of the LNBP10 datasheet.

In regards to claim 4, the modified circuit of LNBP10 in view of Vizer's teachings does not disclose the use of buck converter for the switch-mode power supply.

Official notice is taken that the buck converter is a well-known type of DC-DC switch mode power supply used to "step down" the input voltage level to a lower output voltage level.

It would have been obvious to one of ordinary skill to further modify the LNBP10 circuit in view of Vizer's teaching to use a buck converter for the switch mode power supply where the highest required output voltage level is lower than the supply voltage. The motivation is to provide means to "step-down" the input voltage.

In regards to claim 5 and method claim 10, the modified circuit of LNBP10 in view of Vizer's teachings does not disclose the use of boost converter for the switch-mode power supply.

Official notice is taken that the boost converter is a well-known type of DC-DC switch mode power supply used to "step up" the input voltage to a higher output voltage level.

It would have been obvious to one of ordinary skill to further modify the LNBP10 circuit in view of Vizer's teaching to use a boost converter for the switch mode power supply where the lowest required output voltage level is higher than the supply voltage. The motivation is to provide means to "step-up" the input voltage.

In regards to claim 6 the modified system of LNBP10 in view of Vizer's teachings, the linear amplifier comprises a first output port portion (LNBA) and a second output port portion (LNBB), where the output of the linear amplifier is provided at a selected one of the output port portions in response to an output port control signal (OSEL). Note column 1 in page 1, chart in page 3, and truth table in page 4 of the LNBP10 datasheet.

In regards to claim 11, note claims 1 and 3.

4. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over "LNBP10 Series LNBP20" datasheet (henceforth referred to as LNBP10), published in September 1998 by ST Microelectronics in view of Vizer (US Pat. 5,893,023) as applied to claim 11 above and in further view of Mammano et al. (US Pat. 5,422,562).

In regards to claim 12, the modified LNBP10 circuit in view of Vizer's teaching lacks the recited limitations in the switch mode power supply.

Mammano et al. shows a standard mode power supply comprising an error amp (34), where the first input is coupled to a reference voltage (V_{REF}) and a feedback input that is responsive to the output of the power supply (20); a

pulse width modulation comparator (16) responsive to the output of the error amp for controlling a transistor (14); a transistor (14) where the first input is coupled to the input voltage source (18), the control port is coupled to the PWM comparator (16), and the third terminal is coupled to the inductor (24); an inductor (24) where the first terminal is coupled to the third terminal of the transistor (14) and the output of the linear regulator (V_O) is provided at the second terminal. Note figure 2 in Mammano et al.

It would have been obvious to one of ordinary skill in the art at the time of invention to further modify the LNBP10 circuit modified in view of Vizer to use the switch mode power supply of Mammano et al. in order to provide a switching regulator with an improved dynamic response as specifically taught by Mammano et al. (see column 1, lines 6-9). Further more, only the internal circuit of the switch-mode power supply is modified without changing its interface. Therefore, the switch-mode power supply still comprises an input port to which an input voltage source is connected, a control port, to which a reference voltage is connected, and an output port, which supplies the regulated output to the linear amplifier.

In regards to claim 14, the PWM of Mammano et al. is a current mode PWM. Therefore the modification of LNBP22 in view of Mammano et al. is a current mode PWM as well. Note column 4, lines 10-13.

In regards to claim 13, the LNBP10 circuit modified in view of Vizer lacks an offset voltage generator coupled between the reference voltage and the first input of the error amplifier.

It is well know that the error amplifier functions by comparing the reference voltage to the feedback input voltage, generating an output signal proportional to the difference, which in turn controls the duty cycle of the PWM comparator to regulate the output voltage. The output voltage is "regulated" when the feedback voltage level equals the reference voltage level, i.e. the output voltage level is at the value determined by the reference voltage level. Therefore the desired value of a "regulated" output is directly proportional to the reference voltage, i.e. to increase the value of a desired output, the reference voltage must be increased. If it is desired that the switch mode power supply regulate a higher voltage to be transmitted to the linear amplifier, an offset voltage can be added between the reference voltage and the first input o the error amplifier.

Therefore it would have been obvious to add an offset voltage generator between the first input of the error amplifier and the reference voltage in order to increase the output voltage of the switch mode power supply by a predetermined value.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Usha Raman whose telephone number is (571) 272-7380. The examiner can normally be reached on Mon-Fri: 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Faile can be reached on (571) 272-7375. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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